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EXAMINER	
SALL, EL HADJI MALICK	
ART UNIT	**PAPER NUMBER**
2157	

DATE MAILED: 09/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/818,062	HARIDAS ET AL.	
	Examiner	Art Unit	
	El Hadji M Sall	2157	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- *Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.*
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. ***DETAILED ACTION***

This action is responsive to the application filed on March 26, 2001. Claims 1 - 25 are pending. Claims 1 - 25 represent method and system for a voice multicast hardware accelerator.

2. ***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-2, 6-7, 11-12, and 21-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaka U.S. 6,654,455 in view of Iwama et al. U.S. 6,600,735.

Isaka teaches the invention substantially as claimed including IP conference telephone compatible with IP-PBX systems (see abstract).

As to claim 1, Isaka teaches in a network device including a host system coupled to a memory to store data and a line card to interface with a plurality of user devices, a method comprising:

receiving a network packet including voice data by the host system (column 1, lines 57-62, Isaka discloses a conference trunk is interconnected to the highway for performing, upon receiving packets...);

sending a voice packet related to the voice data to the line card without duplication, the voice packet including descriptor fields for multicasting the voice data

(column 1, lines 62-65, Isaka discloses the at least three telephone terminal systems connected for a conference send packets of voice signals received from the telephone terminals to the network to address them to the conference trunk; column 7, lines 60-65, Isaka discloses...a multicast router 70 is substituted...; column 7, lines 26-32, Isaka discloses...each receives the above voice packets via the IP network 10, and each analyze the headers of the packets...the CPU 40 identifies a packet meant for the telephone...) ;

selectively multicasting the voice data to the plurality of user devices based on the descriptor fields in the voice packet (column 2, lines 45-49, Isaka discloses each IP telephone 12 is a telephone terminal...capable of selectively assembling a voice signal into an IP packet and sending the packet to the IP network 10 or disassembling a received IP packet to thereby reproduces a voice signal; column 7, lines 65-67, Isaka discloses the multicast router 70 manages an IP multicast group that may be set up in the IP network 10a; column 7, lines 26-32, Isaka discloses...each receives the above voice packets via the IP network 10, and each analyze the headers of the packets...the CPU 40 identifies a packet meant for the telephone...);

Isaka fails to teach storing the voice data in the memory; and selectively multicasting the voice data stored in the memory to the plurality of user devices based on the descriptor field in the voice packet.

However, Iwama teaches Internet telephone connection method, bandwidth controller and gate keeper. Iwama teaches storing the voice data in the memory (figure 9; column 14,lines 13-23, Iwama discloses figure 9 is functional block diagram showing a voice relay router...the storage device (1802) is a memory device such as RAM or the like which is contained in the router).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Isaka in view of Iwama to store the voice data in the memory of the multicast router; and selectively multicasting the voice data stored in the memory to the plurality of user devices based on the descriptor field in the voice packet. One would be motivated to do so to monitor communication quality under bandwidth reservation (see abstract).

As to claim 2, Isaka teaches the method of claim 1, wherein the receiving of the network packet includes receiving an Internet Protocol (IP) packet having the voice data (column 2, lines 45-49, Isaka discloses each IP telephone 12 is a telephone terminal...capable of selectively assembling a voice signal into an IP packet and sending the packet to the IP network 10 or disassembling a received IP packet to thereby reproduces a voice signal).

Claims 6-7, 11-12, and 21-22 do not teach or define any new limitations above claims 1-2 and therefore are rejected for similar reasons.

4. Claims 3, 8, 13, 19, and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaka U.S. 6,654,455, in view of Iwama et al. U.S. 6,600,735, and further in view of Onishi et al. U.S. 5,434,863.

Isaka teaches the invention substantially as claimed including IP conference telephone compatible with IP-PBX systems (see abstract).

As to claim 3, Isaka teaches the method of claim 1.

Isaka fails to teach the method of claim 1, wherein the descriptor fields include a memory pointer field, status field, or a data length field.

However, Onishi teaches internetworking apparatus for connecting plural network systems and communication network system composed of plural network systems mutually connected. Onishi teaches the descriptor fields include a memory pointer field, status field, mask field, or a data length field (figure 14; column 7, lines 66-68 – column 8, lines 1-4, Onishi discloses...a routing table 400 is made up of a field 401 of an IP address for representing the destination network, subnet mask data 402 for representing subnet information of the destination network...).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Isaka in view of Onishi to include in the descriptor fields a memory pointer field, status field, mask field, or a data length field. One would be motivated to do so to identify the routing information.

Claims 8, 13, 19, and 23 do not teach or define any new limitations above claims 3 and therefore are rejected for similar reasons.

5. Claim 4-5, 9-10, 14, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaka U.S. 6,654,455 in view of Iwama et al. U.S. 6,600,735, in view of Onishi et al. U.S. 5,434,863, and further in view of Lin et al. U.S. 6,651,225.

Isaka teaches the invention substantially as claimed including IP conference telephone compatible with IP-PBX systems (see abstract).

As to claim 4, Isaka teaches the method of claim 3, wherein the selective multicasting of the voice data include sending the voice data to selected user devices (column 2, lines 45-49, Isaka discloses each IP telephone 12 is a telephone terminal...capable of selectively assembling a voice signal into an IP packet and sending the packet to the IP network 10 or disassembling a received IP packet to thereby reproduces a voice signal; column 7, lines 65-67, Isaka discloses the multicast router 70 manages an IP multicast group that may be set up in the IP network 10a; column 7, lines 26-32, Isaka discloses...each receives the above voice packets via the IP network 10, and each analyze the headers of the packets...the CPU 40 identifies a packet meant for the telephone...).

Isaka fails to teach multicast hardware accelerator is used to send the voice data to selected user devices based on the mask field.

However, Lin teaches dynamic evaluation logic system and method. Lin teaches a hardware accelerator (figure 2, item 120).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Isaka in view of Lin to use multicast hardware accelerator to send the voice data to selected user devices based on the mask field. One would be motivated to do so to allow multiple users doing interactive operations in a manner that allows each user to shift back and forth between hardware emulation and software simulation to discover and eliminate problems in the IC design.

As to claim 5, Isaka teaches the method of claim 4.

Isaka fails to teach the multicast hardware accelerator includes a field programmable gate array (FPGA) device.

However, Lin teaches hardware accelerator includes a field programmable gate array (FPGA) device (column 42, lines 19-24, Lin discloses The RCC Hardware accelerator 2620, which is also referred to as the RCC Array in other sections of this patent specification, contains the reconfigurable array of logic elements (e.g.,FPGA) that can model at least a portion of the user's design in hardware so that the user can accelerate the debugging process).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Isaka in view of Lin to provide a field programmable gate array (FPGA) device in the multicast hardware accelerator. One would be motivated to do so to allow the propagation detector in the FPGA chip alerts the global control unit of any input data that is currently propagating within the FPGA chips (see abstract).

Claims 9-10, 14, and 24-25 do not teach or define any new limitations above claims 4-5 and therefore are rejected for similar reasons.

6. Claim 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Isaka U.S. 6,654,455, in view of Iwama et al. U.S. 6,600,735, and further in view of Lin et al. U.S. 6,651,225.

Isaka teaches the invention substantially as claimed including IP conference telephone compatible with IP-PBX systems (see abstract).

As to claim 16, Isaka teaches a network device comprising:

a host system including a host central processing unit (CPU) and an operating system, the host system to process packet from the network (figure 5, item 70); and

a line card having a plurality of ports to interface to users devices to multicast data (column 1, lines 62-65, Isaka discloses the at least three telephone terminal systems connected for a conference send packets of voice signals received from the telephone terminals to the network to address them to the conference trunk; column 7, lines 60-65, Isaka discloses...a multicast router 70 is substituted...; column 7, lines 26-32, Isaka discloses...each receives the above voice packets via the IP network 10, and each analyze the headers of the packets...the CPU 40 identifies a packet meant for the telephone...).

Isaka fails to teach a buffer memory to store data from processed packet by the host system.

However, Iwama teaches a buffer memory to store data from processed packets by the host system (figure 9; column 14,lines 13-23, Iwama discloses figure 9 is functional block diagram showing a voice relay router...the storage device (1802) is a memory device such as RAM or the like which is contained in the router).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Isaka in view of Iwama to introduce a buffer memory to store data from processed packet by the host system. One would be motivated to do so to retain information as close to the input/output loop as possible to reduce access time.

Isaka fails to teach a multicast hardware accelerator to multicast data stored in the buffer memory.

However, Lin teaches hardware accelerator (figure 2, item 120).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Isaka in view of Lin to provide a multicast hardware accelerator to multicast data stored in the buffer memory. One would be motivated to do so to allow multiple users doing interactive operations in a manner that allows each user to shift back and forth between hardware emulation and software simulation to discover and eliminate problems in the IC design.

As to claim 17, Isaka teaches the network device of claim 16.

Isaka fails to teach the multicast hardware accelerator includes a field programmable gate array (FPGA) device.

However, Lin teaches dynamic evaluation logic system and method. Lin teaches hardware accelerator includes a field programmable gate array (FPGA) device (column 42, lines 19-24, Lin discloses The RCC Hardware accelerator 2620, which is also referred to as the RCC Array in other sections of this patent specification, contains the Reconfigurable array of logic elements (e.g.,FPGA) that can model at least a portion of the user's design in hardware so that the user can accelerate the debugging process).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Isaka in view of Lin to provide the multicast hardware accelerator includes a field programmable gate array (FPGA) device. One would be motivated to do so to allow the propagation detector in the FPGA chip alerts the global control unit of any input data that is currently propagating within the FPGA chips (see abstract).

As to claim 18, Isaka teaches the network device of claim 16, wherein the host system is to send a packet relating to the data stored in the buffer memory, the packet includes descriptor fields used to multicast the data stored in the buffer memory (column 2, lines 45-49, Isaka discloses each IP telephone 12 is a telephone terminal...capable of selectively assembling a voice signal into an IP packet and sending the packet to the

IP network 10 or disassembling a received IP packet to thereby reproduces a voice signal; column 7, lines 65-67, Isaka discloses the multicast router 70 manages an IP multicast group that may be set up in the IP network 10a; column 7, lines 26-32, Isaka discloses...each receives the above voice packets via the IP network 10, and each analyze the headers of the packets...the CPU 40 identifies a packet meant for the telephone...);

As to claim 20, Isaka teaches the network device of claim 16.

Isaka fails to teach the data stored in the buffer memory includes voice data.

However, Iwama teaches the data stored in the buffer memory includes voice data (figure 9; column 14,lines 13-23, Iwama discloses figure 9 is functional block diagram showing a voice relay router...the storage device (1802) is a memory device such as RAM or the like which is contained in the router).

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Isaka in view of Iwama to introduce a buffer memory to store data from processed packet by the host system. One would be motivated to do so to retain information as close to the input/output loop as possible to reduce access time.

Isaka fails to teach the voice data is to be multicasted by the multicast hardware accelerator.

However, Lin teaches a hardware accelerator (figure 2, item 120)

It would have been obvious to one of ordinary skill in the art at the time of the invention to modify Isaka in view of Lin to provide a multicast hardware accelerator to multicast data stored in the buffer memory. One would be motivated to do so to allow multiple users doing interactive operations in a manner that allows each user to shift back and forth between hardware emulation and software simulation to discover and eliminate problems in the IC design.

7. Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to El Hadji M Sall whose telephone number is 703-306-4153. The examiner can normally be reached on 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ario Etienne can be reached on 703 308-7562. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

El Hadji Sall
Patent Examiner
Art Unit: 2157

SALEH NAJJAR
PRIMARY EXAMINER